Advancing AI for EDA: from Supervised Learning to Circuit Foundation Models

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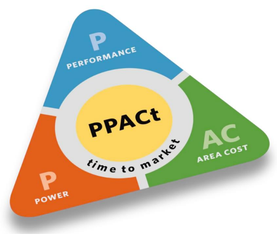
Overview

❖ **Method: AI for EDA paradigm shift**

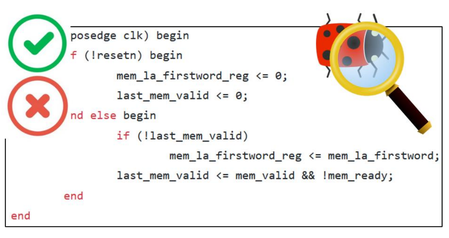
➢ **Tradition: task-specific supervised** learning

➢ **New trend: general** Circuit Foundation Model

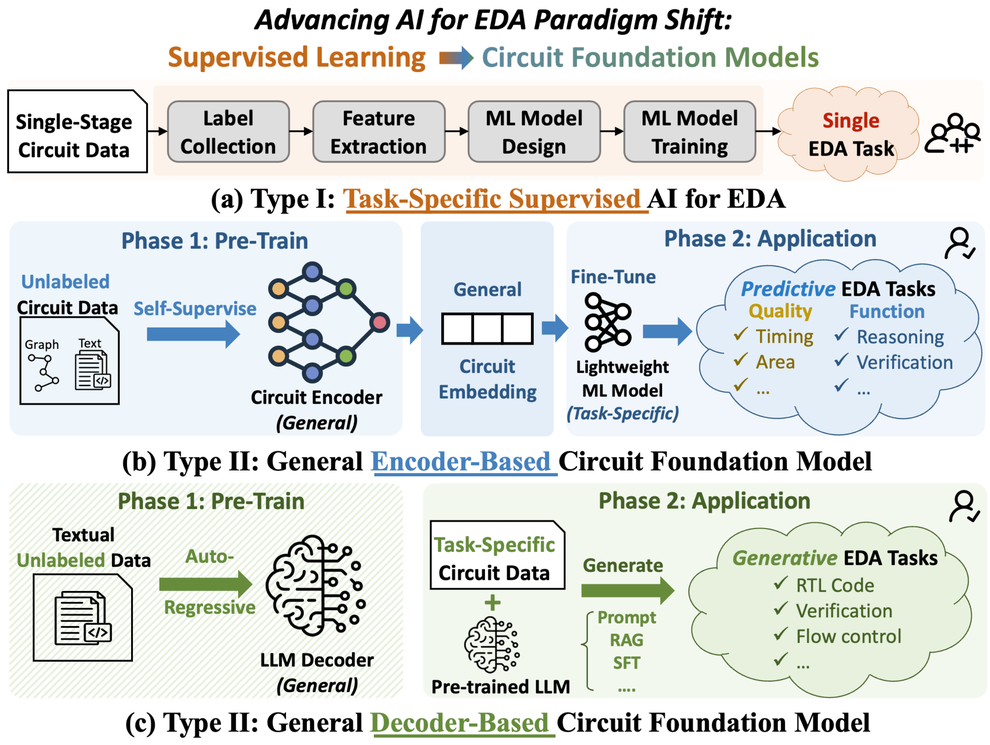
❖ **Application: key VLSI objectives**



Design Quality
PPA eval. & opt.



Functionality
Correctness Verification



My Works
in top-tier EDA/AI venues

Year		
2023	WASIM [TCAD'23] MasterRTL [ICCAD'23/TCAD'24] RTL-Timer [DAC'24]	1. Task-specific: RTL Formal Verification & PPA Evaluation
2024		
2025	CircuitEncoder [ASP-DAC'25] CircuitFusion [ICLR'25] NetTAG [DAC'25]	2. CFM-Encoder: Multimodal RTL & Netlist General Encoders
	AssertLLM [ASP-DAC'25] GenEDA [ICCAD'25]	3. CFM-Decoder: LLM Decoder & Encoder -Decoder Alignment

Type I: Supervised Learning → Type II: General Circuit Foundation Models

❖ RTL PPA Evaluation & Optimization

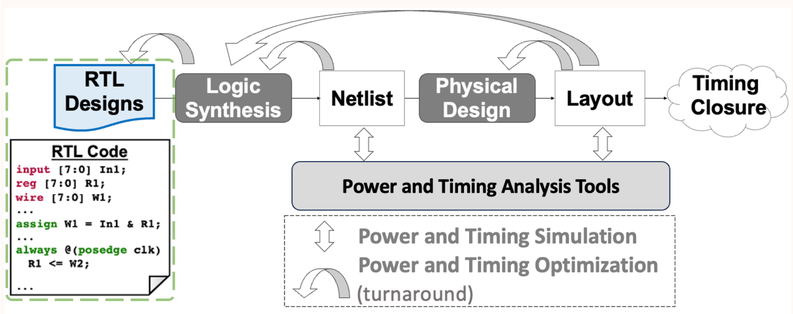
Highlights

➢ **MasterRTL** [ICCAD'23/TCAD'24]

- **Coarse-grained** overall PPA evaluation

➢ **RTL-Timer** [DAC'24]

- **Fine-grained** RTL register slack prediction
- Enable early timing **optimization**



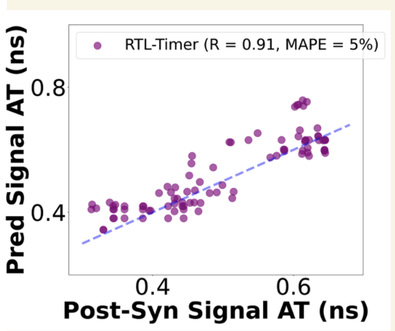
Key Method

- RTL as **Boolean operator graphs**
- **Feature engineering** for PPA
- **Multi-level ML** models for PPA

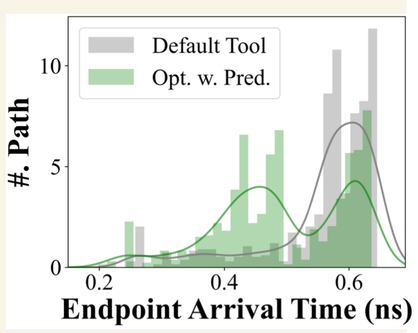
✓EDA Task: PPA Prediction for Opt

Type	Method	Slack R	Slack MAPE	WNS R	WNS MAPE	TNS R	TNS MAPE	Power R	Power MAPE	Area R	Area MAPE
Hardware Task-Specific	**RTL-Timer**	0.85	17%	0.9	16%	0.96	25%	N/A		N/A	
	MasterRTL	N/A		0.89	18%	0.94	28%	0.89	26%	0.98	16%
	SNS v2	N/A		0.82	22%	N/A		0.76	28%	0.93	25%
Text Encoder	NV-Embed-v1	N/A		0.49	17%	0.97	55%	0.85	44%	0.86	24%
Software Encoder	UnixCoder	N/A		0.46	21%	0.95	44%	0.83	29%	0.85	26%
	CodeT5+ Encoder	N/A		0.55	21%	0.63	43%	0.49	46%	0.45	39%
	CodeSage	N/A		0.23	25%	0.86	45%	0.8	38%	0.77	41%
RTL Encoder	**CircuitFusion**	**0.87**	**12%**	**0.91**	**11%**	**0.99**	**15%**	**0.99**	**13%**	**0.99**	**11%**

High **correlation** in prediction



Better **timing distribution**

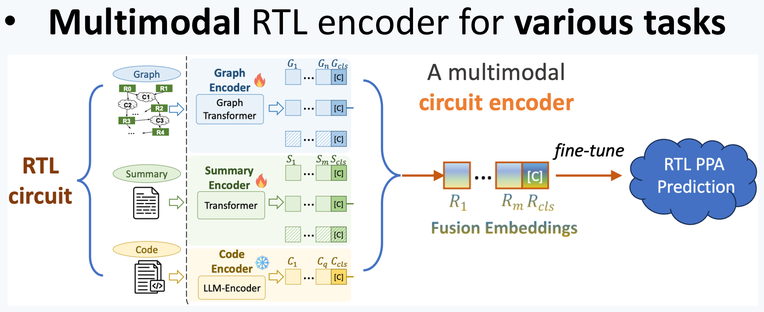


❖ General RTL & Netlist Encoder

Highlights

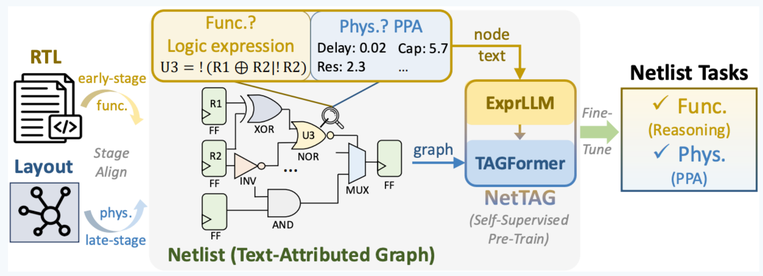
➢ **CircuitFusion** [ICLR'25]

- **Multimodal** RTL encoder for **various tasks**



➢ **NetTAG** [DAC'25]

- **Multimodal** netlist encoder for **various tasks**



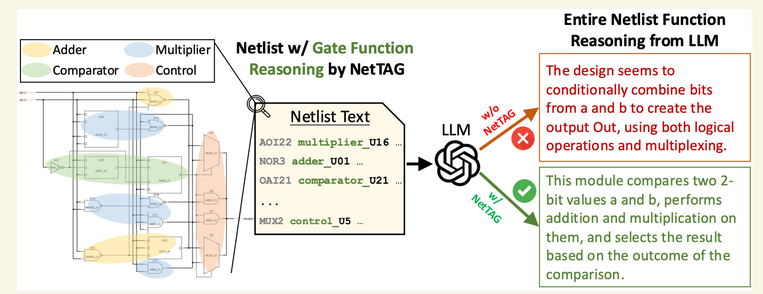
➢ **CircuitEncoder** [ASP-DAC'25]

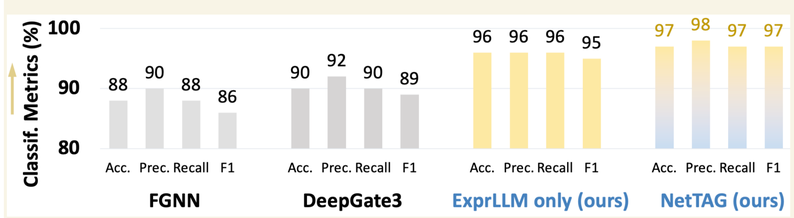
- Align **cross-stage** RTL-netlist encoder

Key Method: pretrain-finetune paradigm

- Circuit multimodal self-supervised learning
- Cross-stage RTL-netlist-layout alignment

✓EDA Task: Functional Reasoning



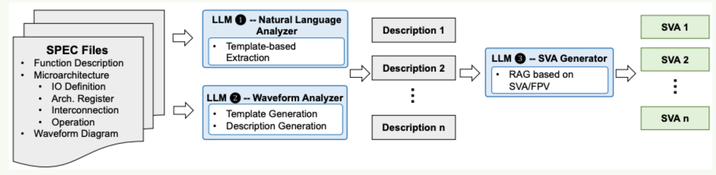


❖ LLM for Assertion Generation

Highlights

➢ **AssertLLM** [ASP-DAC'25]

- Automate **assertion** generation from spec

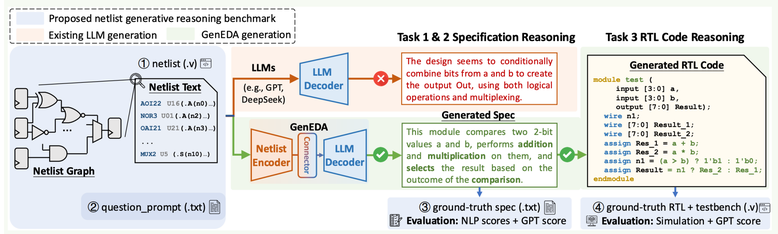


❖ Bridge Encoder & LLM Decoder

Highlights

➢ **GenEDA** [ICCAD'25]

- Encoder-Decoder with **connectors**
- Enable **generative** function reasoning



➢ Publications (first-author)

[1] **W. Fang**, et al. "GenEDA: Towards Generative Netlist Functional Reasoning via Cross-Modal Circuit Encoder-Decoder Alignment." in **ICCAD**, 2025.

[2] **W. Fang**, et al. "NetTAG: A Multimodal RTL-and-Layout-Aligned Netlist Foundation Model via Text-Attributed Graph." in **DAC**, 2025

[3] **W. Fang**, et al. "CircuitFusion: Multimodal Circuit Representation Learning for Agile Chip Design." in **ICLR**, 2025

[4] **W. Fang**, et al. "A Self-Supervised, Pre-Trained, and Cross-Stage-Aligned Circuit Encoder Provides a Foundation for Various Design Tasks." in **ASP-DAC**, 2025

[5] **W. Fang**, et al. "Transferable Pre-Synthesis PPA Estimation for RTL Designs With Data Augmentation Techniques." in **TCAD**, 2024

[6] **W. Fang**, et al. "Annotating Slack Directly on Your Verilog: Fine-Grained RTL Timing Evaluation for Early Optimization." in **DAC**, 2024

[7] **W. Fang**, et al. "MasterRTL: A Pre-Synthesis PPA Estimation Framework for Any RTL Design." in **ICCAD**, 2023

[8] **W. Fang**, et al. "r-map: Relating Implementation and Specification in Hardware Refinement Checking." in **TCAD**, 2023

[9] Z. Yan*, **W. Fang***, et al. "A Self-Supervised, Pre-Trained, and Cross-Stage-Aligned Circuit Encoder Provides a Foundation for Various Design Tasks." in **ASP-DAC**, 2025

[10] **W. Fang**, et al. "A Survey of Circuit Foundation Model: Foundation AI Models for VLSI Circuit Design and EDA." in **TODAES**, under review.

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About me